HIGH DENSITY MICROELECTRONICS PACKAGING ROADMAP FOR SPACE APPLICATIONS

Lissa Galbraith, PhD
Jet Propulsion Laboratory, California Institute of Technology
Mail Stop 125-152, 4800 Oak Grove Drive, Pasadena, CA 91109-8099, USA

ABSTRACT

High density interconnect microelectronics emphasizes the effective integration of several critical and complex electronic packages and technologies. This Roadmap introduces current technologies in use, related strategic issues and trends, and research recommendations for space applications. Electronic packages are optimized for low cost, portability, robustness, high speed, power efficiency, and for small size and low weight. Satisfying these increasing demands will require enhanced electronic performance with an associated improvement in packaging performance and better relief from thermal and mechanical stresses.

Technical challenges and directions for high density interconnect microelectronics packaging include understanding latent electromigration and dendritic growth, multilayer board hole wall wicking reliability issues, and characterization of reworkable inexpensive underfill. Current research directions include Vertical Cavity Surface Emitting Laser (VCSEL) packaging for low cost optical interconnects, high density vias, and stencil printing with conductive adhesives for direct chip attach. Technology challenges are described first for components. Forecasts and recommendations for research direction are given for components, materials, and packaging.

Key Words: microelectronic packaging, roadmap, trends, forecasts

TECHNOLOGY CHALLENGES AND RESEARCH RECOMMENDATIONS

Optoelectronics

The traditional hierarchical network topology of circuit switching will need to evolve to a flat network topology for packet switching which is more conducive to data and Internet traffic. Technology development required to support this includes single tunable lasers to replace multiple fixed wavelength lasers, ultrawide bandwidth fibers and optical amplifiers, and large capacity optical cross connects and routers for handling multi-terabit information rates on a single fiber. Also needed is the development of 13 GHz laser drivers and amplifiers, evolving 10Gb/s to be as affordable as 2.5Gb/s in general, defining standard interfaces for 10Gb/s metallic or fiber, as well as further development of receivers and transmitters to use wave division multiplexing for 10Gb/s traffic.

Managing Thermal Stress

Heat removal is essential for an electronic package to obtain optimal performance without failure. The substrate and circuit often possess different rates of thermal expansion. There may be stresses at the locations where two materials interact, i.e., interconnections. These stresses can lead to a break in connections and package failure. Many packaging technologies have been tested for addressing these problems. Appropriate interconnection materials with similar coefficients of thermal expansion (CTE) are being examined. Silicon carbide in aluminum is being investigated as a material for finned heat sinks. It has a comparable CTE to that of silicon, is light weight and has high thermal conductivity. Flexible substrates also show promise.

Air-cooling is a popular technique because it is inexpensive, light, and portable. By placing a potential difference between two connected dissimilar metals, one metal becomes cool while the other increases in temperature. This design allows one side to cool the chip while the other side dissipates the heat through a heat sink. Designs incorporating air-cooling are improving performance ever year. Liquid cooling is effective, but is expensive, heavy, and requires self-containment. The NASA Electronic Parts and Packaging Program is examining several issues within extreme environments including interconnect reliability of cold electroncs and packaging of high-temperature SiC-based electronics.

High Density Interconnect Microelectronics Packaging

The ever increasing density of interconnects offers many opportunities as well as challenges. Latent electromigration and dendritic growth continue to plague packaging miniaturization. Multilayer board hole wall wicking reliability needs improvement. Characterization of reworkable inexpensive underfill is another area worthy of further research. Some work is beginning on the search for cost-effective low-noise controlled impedance packaging for massively wide bussing at GHz frequencies utilizing very high density interconnect (VHDI) system in a package (SIP) designs. There is also a need for increased reliability of vertical cavity surface emitting laser (VCSEL) devices. The NASA Electronic Parts and Packaging Program is

investigating the enhanced reliability of microelectronic circuit interconnects using microwave radiation.

Solder voids continue to jeopardize reliability. The location and size of a solder ball void is an important factor in determining potential defect impact. Large voids in the interconnect area between the ball and the package are more likely to cause functional defects than small voids near the board. Overall size appears to be more important than total volume. Several small voids may improve fatigue resistance, while a single large void may cause failure. Problems associated with voids include reduced fatigue resistance and causing the ball to separate from the package. Among the factors affecting board level reliability in solder ball array packages are board finish, solder paste selection and application, and reflow cycle [15].

A major difficulty with chip scale and near chip scale packages is that these substrates are often much thinner and many of the solder joints are directly beneath the die, with a very different CTE than that of the substrate [5]. A complicating issue is that these packages have a fine ball pitch (0.5 mm -- 0.8 mm). The significantly smaller solder ball diameter may result in higher thermal stress concentrated in a smaller solder joint. One design being investigated is an enhanced BGA package with cavity up orientation and a stiffened flex circuit leadframe structure. This design appears to have comparable reliability, thermal, and electrical performance to other flex only and laminate-based packages such as plastic BGAs and CSPs [5].

Flip Chip Packaging

One problem facing the flip chip foundries is the availability of high yield, high reliability, flexible and cost-effective equipment to accommodate the extremely varied flip chip bumped processing needs. The flip chip market is expected to grow to 2.4 billion units in 2004. The chip packaging foundries need new packaging processes that are capable of performing to the higher standards of reliability demanded by high density packaging for bump processing. The high-resolution precisely controlled focus mechanisms typically found in stepper technology need to be investigated for processing high-resolution, thin-film photo resists. This high precision focus control often limits the total range of focus positioning to approximately 10 microns, making it difficult to adjust the focus over the broader range required on thick films, particularly those in excess of 40 to 50 microns [14].

There are several elements of the laminate assembly process requiring optimization including substrate dehydration, underfill dispensing and flow, and underfill curing. Research should also continue on underfill materials characterization and optimization.

Some of the underfill materials characterization needing further detail include:

- Optimal curing temperature range
- Coefficient of thermal expansion
- Glass transition temperature
- Moisture uptake
- Flow rate
- Modulus of elasticity over a range of temperatures (-55 to +110 °C)
- Shear force at dry conditions
- Percentage drop of shear force with temperature and humidity
- Compliant coating versus hermetic sealing of Chip On Board (COB) die.

Materials Characterization

Materials characterization is an expansive subject ripe with issues to be resolved One area warranting further investigation is transducers of polymer thick film (PTF) with silicon. Amorphous semiconductor materials for programmable switching interconnections and buried R/C/L circuit element fabrication is another topic under review. **A** superconducting substrate for multichip module (MCM) technology being examined is the yttrium-barium-copper-oxide yttrium-stabilized zirconia multilayer substrate [6] .

The investigation of multilayered wiring and direct chip attach packaging continues to be of interest in an effort to minimize the effect of CTE mismatch between the IC chip and substrate. Some of the materials being investigated for this include carbon cloth, milled fibers, and nanofibers which have many desirable characteristics such as low coefficient of thermal expansion, and a high modulus. Research will continue in this area [13].

There are several critical characteristics of plastic packaging materials for high reliability applications. These include the glass transition temperature, the coefficient of thermal expansion, extractable ionic materials, moderate elastic modulus, and I/O structure. One of the concerns with using commercial off-the-shelf (COTS) ICs is that device data sheets do not always specify all the characteristics of plastic packaging materials of interest for high reliability applications. Often space applications require a higher glass transition temperature than the readily accessible COTS devices can provide. The CTE needs to be balanced between a low expansion IC chip and the high expansion substrate. While the elastic modulus requirements for high reliability applications are often moderate, the modulus needs to be high enough to provide mechanical protection and low enough to absorb interfacial strains. Some of the testing techniques used to a evaluate COTS devices are the following. Differerential scanning calorimetry is used to evaluate the glass transition temperature of a package. The presence of semiconductor or I/O metals

may only affect the magnitude of the signal, not the temperature at which the endotherm peak occurs [4]. Another testing technique under investigation is thermal mechanical analyzing which can be used to determine the overall expansion of the package. Careful separation of plastic, metal, and semiconductor material is required. Dynamic mechanical analysis can be used for modulus determination. Ruggedizing COTS for use in harsh environments is also under investigation. Inorganic chip sealants are being developed for application onto bare die prior to high-pressure molding. New approaches are needed to permit more rapid assessment of COTS for harsh environments and other high reliability applications.

Microelectromechanical Systems (MEMS) Packaging

Two issues facing the MEMS industry are the fragile characteristics of wafers and the need for foundry processes just before packaging. MEMS issues are often application-specific and solutions for one application may not translate to others. There are many space applications of MEMS including accelerometers, microspectrophotometers, gyroscopes, movable mirrors, chemical analyzers, optical switches, tunable capacitors, infrared imagers, microrelays, and pressure sensors. Extremely accurate package orientation is often a challenge. Skew may reduce sensitivity due to the device not pointing true. Component tilt is also a problem because this would reduce the effective direction of motion and also reduce sensitivity. A thicker solder fillet could reduce compliancy. Optical products require hermetic sealing but also the need to provide a light path. A port hole is designed into the package for movable optical systems which require that the package atmosphere remain clear.

MEMS materials can outgas and generate atmosphere that causes damage after sealing. Hydrogen getters are often used to prevent poisoning of GaAs devices. A solution being investigated uses a hydrogen getter utilizing palladium oxide in combination with zeolite dispersed within a stable polymer matrix [3]. The PdO converts hydrogen gas to water, which is then consumed by the zeolite making the reaction nearly irreversible. Hydrogen sources include the electroplating on the metal package and die attach adhesives.

MEMS integration is another area of issue. MEMS with hybrid thick film and MCM versus monolithic packaging are two such issues. Nonhermetic direct chip attach under-bump metallization can also be contentious. Die level test and handling of multichip packaging (MCP) can also present challenges. Broadband light source reliability is another MEMS integration application needing improvement. The NASA Electronic Parts and Packaging Program is studying the packaging and reliability of MEMS broadband light sources.

CHALLENGES FOR SPACE APPLICATIONS

Managing thermal stress at extreme environments (both hot and cold) has always been a challenge for space applications of microelectronic packaging. The reliability of SiC based electronics for extremely high temperatures is often a concern for space electronics. Long life (10+ years) reliability at extreme cold temperatures is also of interest. Radiation shielding and characterization of component and system sensitivity to radiation are unique concerns to the application of packaging in space. Reliability testing with very small volume production (2-3 total) presents statistical concerns. Should a tested unit be flown? Nondestructive evaluation is of great research interest due to the necessity for very high reliability, very small statistical sample sizes, and the need to minimize redundancy in order to miniaturize the payload.

TECHNOLOGY FORECASTS

The amount invested from June 1999 to June 2000 in commercial space ventures was more than $9 billion dollars. The forecasted growth from 1999 to 2005 for the space industry is 93.3 percent [10]. The satellite services sector is expected to increase to 74.1 billion dollars by 2005 [6]. Data services are expected to increase 513 percent by 2005, along with an increase of 2015 percent in broadband services, with an 414.8 percent increase in remote sensing. The number of spacecraft launched in 1999 was 128. There were 76 commercial payloads and 52 government payloads launched in 1999 [10]. The launch vehicle success rate in 1999 was 89.7 percent with eight countries making launches in 1999.

Figure 1 shows the projected increase in computational power in millions of instructions per second (MIPS). Chip computational power is forecast to be greater than 9,800 MIPS by 2005.

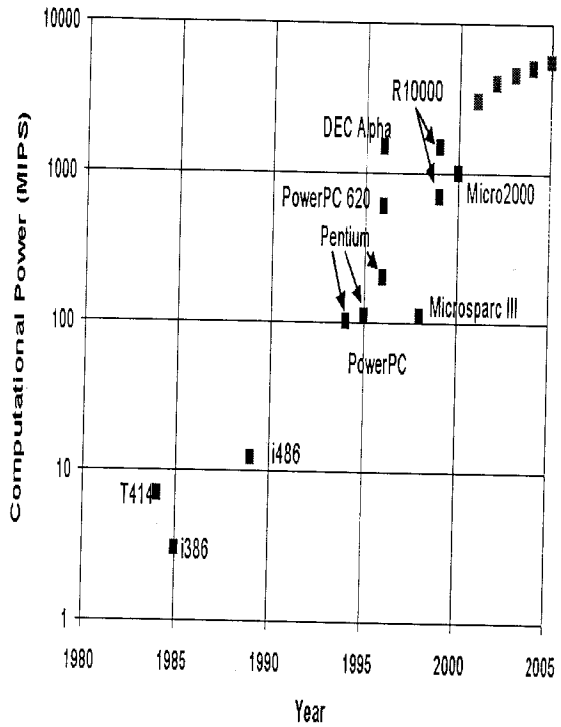

Figure 1. Trends in Computational Power [9]

We are starting to see the merging of ultra-fine pitch, flip chip, and hybrid assembly. This trend is expected to continue. Flip chip in package (FCIP) packaging is expected to increase to 1.7 billion units by 2003. The mean number of I/O interconnects per chip is projected to be greater than 2,500 by 2002. The smallest package feature size will continue to decrease to be less than 0.1 μm by 2005 [10]. The Optoelectronics Industry Development Association has forecast that Internet traffic will surpass voice traffic by the end of 2001 and that voice will be only 1% of network traffic by 2005. Figure 2 shows the trend in thermal management for high density packaging as heat flux in watts/cm^2. Figure 3 shows the mean number of I/O connections per IC since 1990 [12]. Figure 4 plots the trend in packaging density over the years [11]. Figure 5. shows the trend in smallest package feature size in micrometers [11]. Figure 6 shows the chip clock frequency trends of ICs incorporating the same size $AlSiO_2$ interconnects [6].

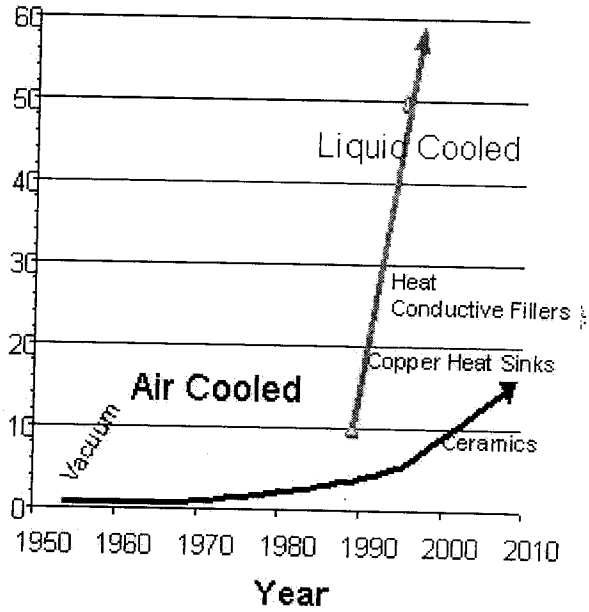

Figure 2. Thermal Management Trends, Heat Flux (watts/cm^2) [11]

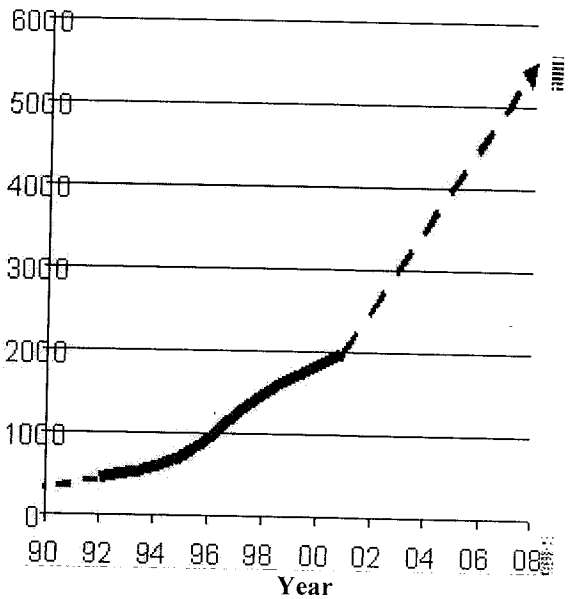

Figure 3. Mean Number of I/O [12]

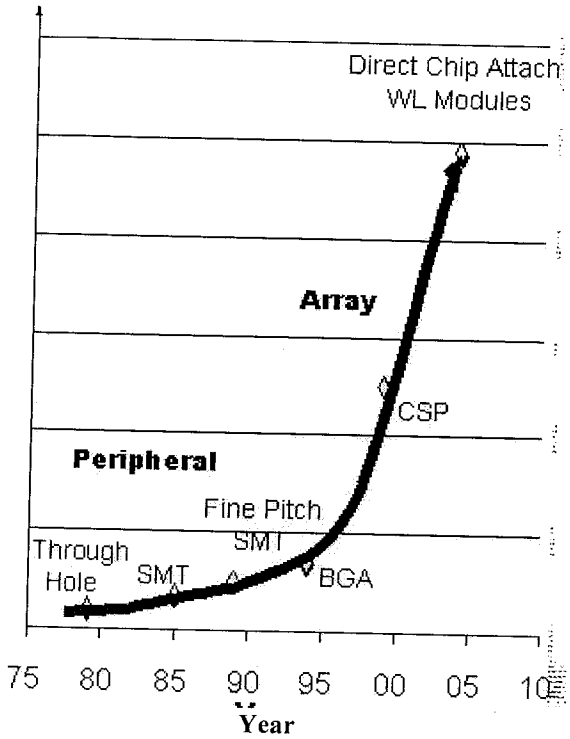

Figure 4. I/O Density of First-Level Packaging [11]

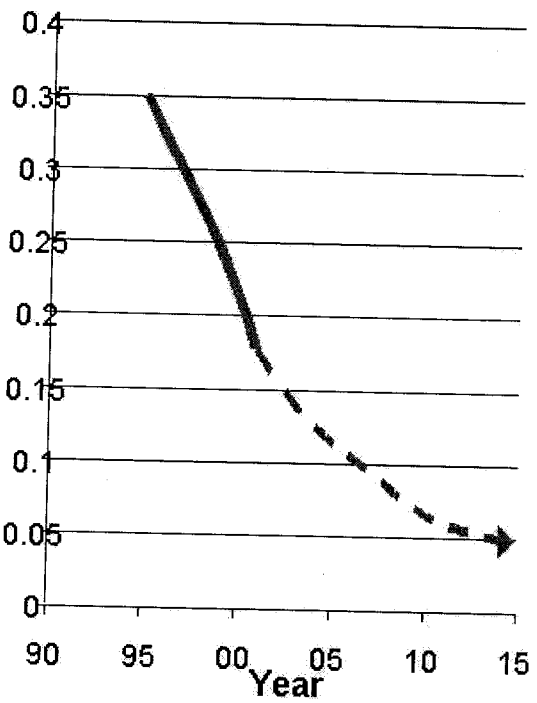

Figure 5. Trend in Smallest Package Feature Size in Micrometers [11]

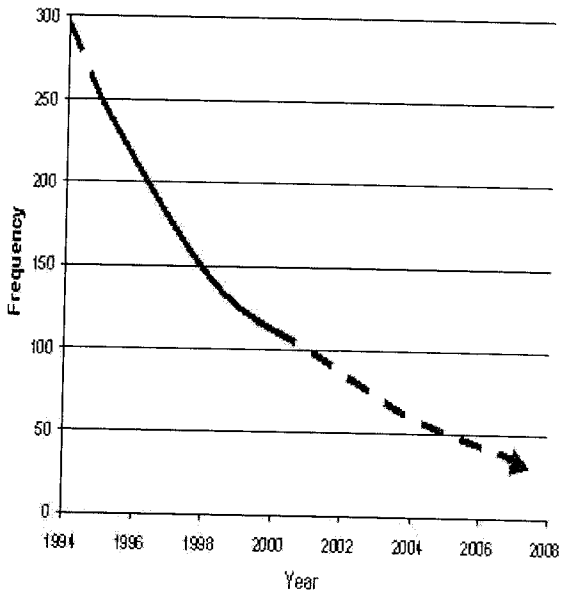

Figure 6. Chip Clock Frequency Trends [6]

CONCLUSIONS

This Roadmap introduced several current technologies in use, related strategic issues and trends, and research recommendations for space applications. There are several areas needing further research emphasis for optoelectronics including single tunable lasers to replace multiple fixed wavelength lasers, ultrawide bandwidth fibers and optical amplifiers, and large capacity optical cross connects and routers for handling multi-terabit information rates on a single fiber. Liquid cooling for thermal management requires more investigation to improve expense and weight. Further characterization of reworkable inexpensive underfill is also needed. Solder voids continue to require investigation. Another topic for continuing research is thermal stress in chip scale package solder balls. There are several elements of the laminate assembly process requiring optimization including substrate dehydration, underfill dispensing and flow, and underfill curing. Amorphous semiconductor materials for programmable switching interconnections and buried R/C/L circuit element fabrication is another area for research. Expanding COTS device data sheets would encourage their investigation for use in high reliability applications. New approaches are needed to permit more rapid assessment of COTS for extreme environments. MEMS packaging concerns include accurate package orientation, integration, and outgassing. Forecasts were presented for computational power, thermal management, I/O density, chip clock frequency, and feature size.

REFERENCES

1. Anberg, D., "Flip Chip Lithography", *Chip Scale Review*, May-June 2000, 44-47

2. Cho, Y..S, C.R. Needles, K.E. Souders, K.W.Hang ,

P.C.Donohue , A.R. Niblett , and D.I.Amey, "LTCC Ceramic Components on Printed Wiring Boards --- The Issues and Potential Solutions", *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston, 665-668

3. Gilleo, K., "MEMS Packaging Issues and Materials", *IMAPS Advancing Microectronics*, Vol. 27, No. 6, Nov-Dec 2000, 9-13

4. Hagge, J.K., "ROBOCOTS: A Program To Assure Robust Packaging Of Commercial Off-The-Shelf (COTS) Integrated Circuits", *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston, 139-149

5. Hayden,, T.F., P.M. Harvey, R.D. Schueller, W.J. Clatanoff, and E. Pyun, "The Performance and Reliability For Cavity-Up Enhanced BGAs", *HDI*, Vol. 3, No. 4, April 2000, 22-31

6. IEEE/SEMI *Proceedings of the Advanced Semiconductor Manufacturing Conference and Workshop: Meeting the Challenges of the Global Marketplace,* September 23-25, 1998, Boston

7. IMAPS, *Proceedings of the International Conference and Exhibition on High Density Interconnect and Systems Packaging*, April 25-28, 2000, Denver

8. IMAPS, *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston

9. Intel web site, 12/18/00, http//:www.intel.com

10. International Space Business Council, "State of the Space Industry", June 2000

11. Klopfenstein, A., Rymaszewski, E., Tummala, R., Editors, *Microelectronics Packaging Handbook*, New York, Chapman and Hall, 1997

12. Luryi, S., Xu, J., Zaslavsky, A., Editors, *Future Trends in Microelectronics:Reflections on the Road to Nanotechnology*, NATO ASI Series E, Vol 323, Boston, Kluwer Academic, 1998

13. Raj, M.P., K. Shinotami, H. Agarwal, G..E. White, and R.R. Ttummala "Evaluation of Carbon-Filled Polymer Composites For Future Base Substrate And Integral Resistor Applications", *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston, 351-356

14. Owens, D.R., and J.K. Lumpp, " PLD and LCVD of Discrete And Microhotplate Tin Oxide Sensors", *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston, 438-442

15. Williams, C. and G. Morrison, " Factors Affecting Board Level Reliability In Solder Ball Array Packages", *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston, 471-476

16. Zs, I.V., J. Pinkola, M. Ruszinko, P. Bojta,, and L. Hertel, " New MCM - L Structure Applying Packageless Chip Size Devices And Laser Processed Board", *Proceedings of IMAPS 2000 International Symposium on Microelectronics*, September 20-22, 2000, Boston, 826-831

ACKNOWLEDGEMENTS

Portions of this work were funded by the NASA Electronic Parts and Packaging Program. Special acknowledgement and appreciation is extended to the following individuals for their contributions and guidance: Rajeshuni Ramesham, PhD, Reza Ghaffarian, PhD, Saverio D'Agostino, Phillip Zulueta, Stephen Bolin, and
Loren Rideout.